Analysis of Risks and Related Damages due to the Implementation of Virtual Metrology Algorithms into Semiconductor Fabrication Lines

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Introduction and motivation

Increasing wafer diameter and decreasing feature sizes demand for reliable and fast process control on wafer level and even within wafer control loops. Virtual Metrology (VM) [1-2] appears to be the only way to reach the required level of control. VM enables the prediction of physical and electrical device parameters on the wafers from information collected in real time from manufacturing tools. Implementing VM algorithms into existing fab structures will permit to virtually measure all processed wafers, thus improving device quality and yield.

A model has been developed to calculate the economic benefits due to the implementation of VM [3-4]. This model has been extended to consider also potential damages in case the VM algorithms fail.

This paper presents the evaluation of potential risks due to the implementation of VM algorithms into existing fabrication lines, providing a valuable and important extension of existing investment assessment.

Identification of risks due to VM

Comprehensive risk analyses were carried out in cooperation with Integrated Device Manufacturers (IDM) using the standardized method of failure mode and effect analysis (FMEA) [3]. The most relevant risks were identified and quantified. Figure 1 gives an overview of the FMEA results. They serve as the basis for calculating potential damages accompanied by failing VM:

- Yield loss due to incorrect VM results.
- Reduced equipment utilization caused by misleading VM results.
- Additional production costs due to “real” metrology steps performed because of failing VM.
- Increased cycle time due to slow trigger signals from VM.

Financial quantification of damages

The potential damages due to failing VM have been calculated based on a 200 mm wafer fab running a 0.13 µm CMOS technology. Default fab and equipment data have been derived from published reports [5]-[7] extendable to sub 40 nm regimes. Failing VM algorithms might lead to the previously mentioned problems which have been discussed with IDMs. Several assumptions were made for the calculations, such as probability of occurrence, yield loss, adjusted sampling rate, time loss, etc. The results of these damage calculations are shown for various process equipment types in Figure 2.

Evaluation of results

As can be depicted from Figure 2, the main contributor for damages is a reduction in yield due to incorrect VM results. Therefore, failure modes causing incorrect VM results have to be treated extensively. Reliable VM algorithms are of major importance for a successful implementation of VM in semiconductor fabrication lines.

Other potential damages were found to be small compared with the potential yield loss. In particular the additional production costs due to increased real metrology steps and the effects of increased cycle time were found to be very small.

When the potential damages of failing VM algorithms are compared with the benefits of implementing VM (see Figure 3-4), it is found that the benefits always exceed the potential damages. The exact results depend on the equipment type which is considered. It seems that VM is especially beneficial for equipment without proceeding regular real metrology step in the process flow.

The calculation of potential damages due to failing VM algorithms can serve as a tool to determine the reliability of VM algorithms which is necessary before VM can be implemented in real factories. The probability of failing VM algorithms seems to be the major parameter affecting the size of potential damages.

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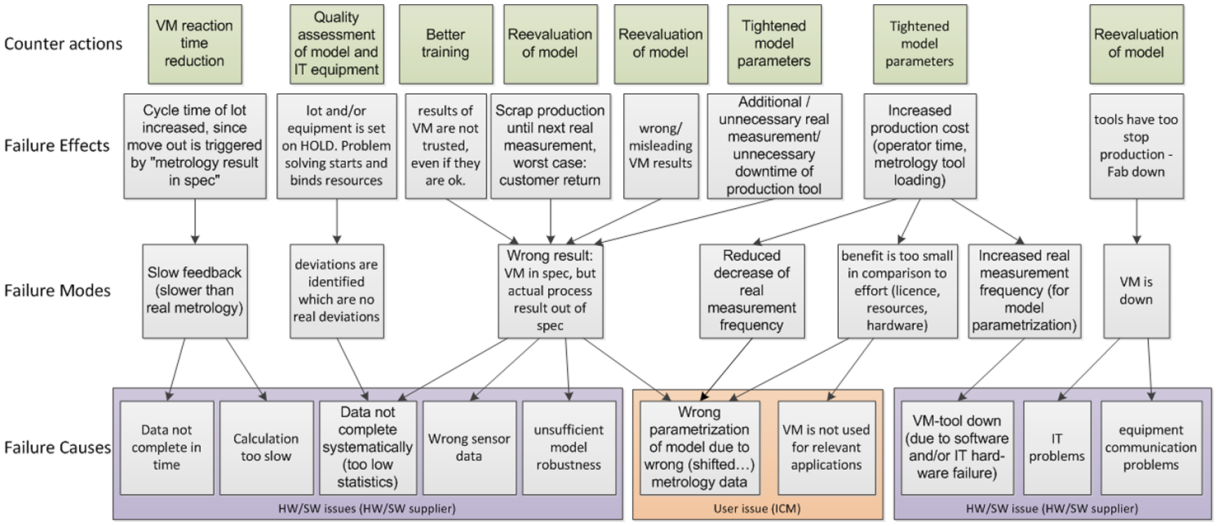

Figure 1: Overview of the most severe VM failure modes and effects identified by FMEA

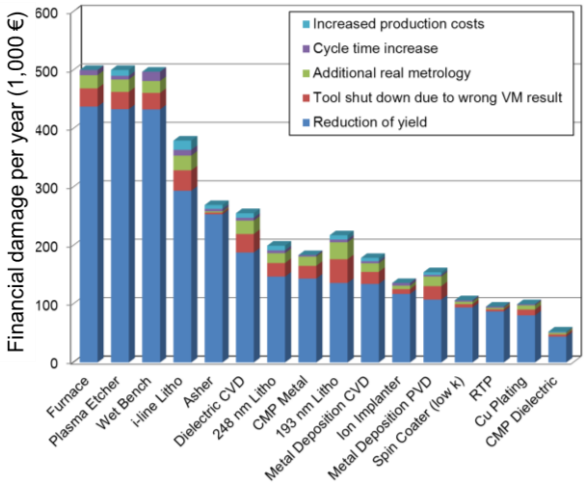

Figure 2: Potential financial damages per year due to failing VM in a model fab for various equipment types

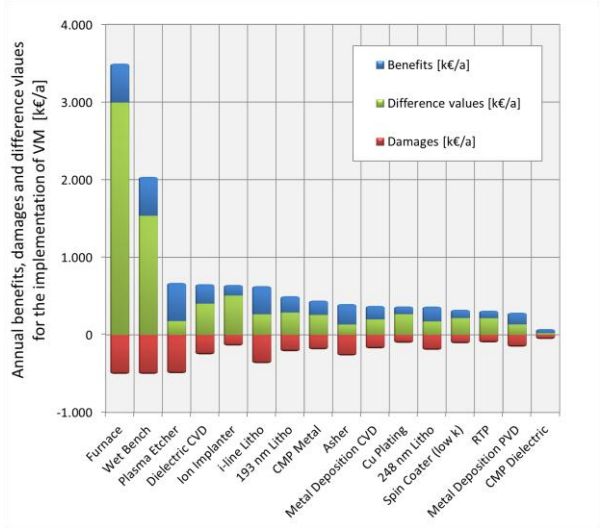

Figure 3: Comparison of benefits and potential damages per year for different equipment types of a model fab

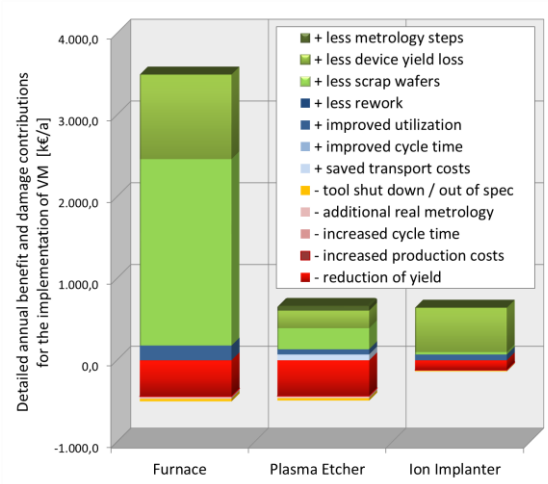

Figure 4: Comparison of detailed benefits and potential damages per year for implementing VM at furnaces, plasma etchers and ion implanters in a model fab

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