

A Calculation Model for the Economic Effects of Implementing Predictive Maintenance Algorithms into Semiconductor Fabrication Lines

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Introduction and motivation

Process tools in leading edge semiconductor facilities represent a huge amount of capital expenditure. It is essential to maximize the use of these assets especially availability and reliability of these tools. Moreover, it is also important to minimize the maintenance costs of these equipment in order to further reduce operational costs of semiconductor fabs. The approach of predictive maintenance (PdM) promises to improve the availability and reliability of semiconductor production tools [1][2]. PdM algorithms forecast the need for maintenance; the corresponding maintenance work is then optimally scheduled and performed before parts fail.

A model has been developed to calculate the economic effects of the implementation of PdM, similar to virtual metrology (VM) [3-4]. The model also considers potential damages in case the PdM algorithms fail.

This paper presents the economic benefits and potential risks due to the implementation of PdM algorithms into existing fab structures, providing a valuable and important extension of existing assessment approaches for such investment.

Economic effects of PdM

The implementation of PdM promises to yield the following effects:

- Reduction of maintenance costs due to focusing on inevitable maintenance actions and optimized timing of the work.
- Increased equipment utilization due to less time reserved for maintenance.
- Reduction of yield losses, scrap wafers and rework due to reduced equipment failures.

The savings and monetary benefits of these effects were calculated in a spreadsheet based model which uses publicly available data [5-7] as default values. These can easily be adapted to fit Integrated Device Manufacturer's (IDM) fabrication lines.

The model calculates also the costs for implementing PdM into the model fab. Costs were

estimated jointly with IDMs considering the experience with similar investment into Advanced Process Control (APC) algorithms. Eventually, the model compares costs to benefits and calculates investment assessment figures such as payback period, return on investment and net present value.

Figure 1 shows the economic benefits due the implementation of PdM at various equipment types. It was found that the potential savings of maintenance costs is an important contributor to the overall benefits. Reduction of scrap wafers is very important for batch equipment, e.g. furnaces because numerous wafers will be scrap, if a major failure occurs. Figure 2 depicts a typical graph for the balance between costs and benefits over time. For several equipment types, payback periods in the range of 1-2 years could be achieved.

Risk analysis

Comprehensive risk analyses were carried out in cooperation with IDMs using the standardized method of failure mode and effect analysis (FMEA) [3]. The most relevant risks were identified and quantified. They serve as the basis for calculating potential financial damages accompanied by failing PdM. Several assumptions were made for the calculations, such as probability of occurrence, increased downtime, increased production costs, etc. The results of these damage calculations are shown for various process equipment types in Figure 3.

Evaluation of results

The calculations for several equipment types result in rather short payback periods. The comparison of benefits with potential damages in case the PdM algorithms fail allows a risk evaluation and the design of appropriate risk mitigation measures. The model can also be used to perform sensitivity analyses to identify those input parameters which have the biggest effect on the results.

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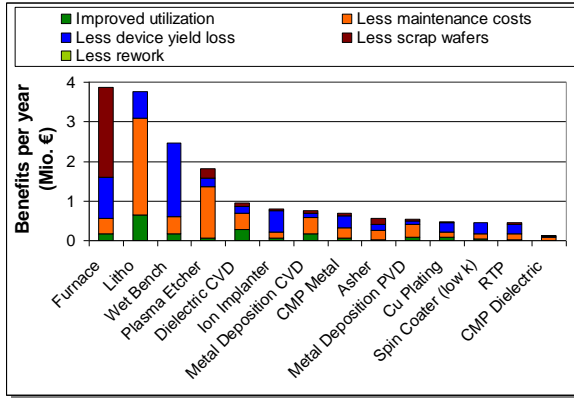


Figure 1: Potential savings due to the implementation of PdM in various equipment types of a 0.13 μm model logic fab

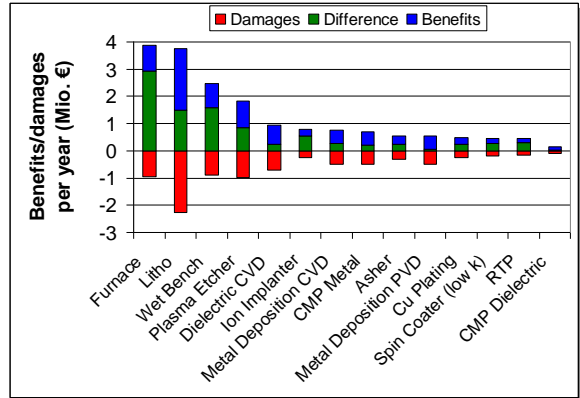


Figure 4: Comparison of benefits and potential damages per year for implementing PdM at various equipment types in a 0.13 μm model logic fab

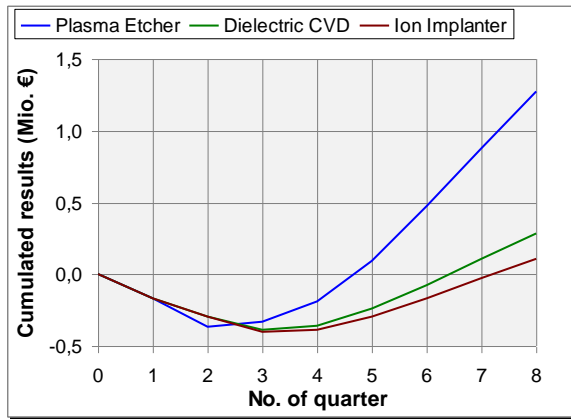


Figure 2: Cumulated results (benefits plus costs) per quarter due to the implementation of PdM at 3 equipment types. Break-even is reached within the 1.25 years (plasma etcher), within 1.75 years (dielectric CVD) and within 2 years (ion implanter)

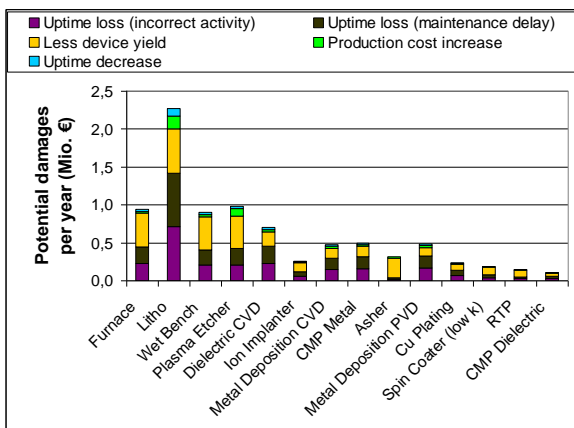


Figure 3: Potential damages per year due to failing PdM in various equipment types of a 0.13 μm model logic fab

References

- [1] K. A. Kaiser and Z. Nagi: *Predictive Maintenance Management Using Sensor-Based Degradation Models*; IEEE Transactions on Systems, Man and Cybernetics – Part A: Systems and Humans, vol. 39. No. 4, July 2009
- [2] M. L. Araiza: *A Formal Framework for Predictive Maintenance*; IEEE Autotestcon, 2004
- [3] M. Koitzsch, J. Merhof, M. Michl, H. Noll, A. Nemecek, A. Honold, et al.: *Implementing virtual metrology into semiconductor production processes - an investment assessment*, Proc. 2011 Winter Sim. Conf., pp. 2017-2028, USA, 2011.
- [4] M. Koitzsch, A. Honold: *Evaluation of economic effects as the basis for assessing the investment into Virtual Metrology*; ISMI Manufacturing Week, AEC/APC Symposium, USA, 2010.
- [5] International Sematech: 130 nm Cu logic process.
- [6] International Sematech: fab model, wafer cost comparison calculator; version 1.0, November 2002.
- [7] International Sematech/Selete: unified equipment performance metrics for 130 nm technology; version 2.0, 300 mm equipment, July 2000.
- [8] M. Koitzsch, A. Honold, H. Noll, A. Nemecek: *Analysis of Risks and Related Damages due to the Implementation of Virtual Metrology Algorithms into Semiconductor Fabrication Lines*; submitted to APC Conference 2012, USA