Evaluation of Economic Effects as the Basis for Assessing Virtual Metrology Investment

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Abstract

This paper presents the evaluation of economic effects due to the implementation of virtual metrology (VM) algorithms into the IT infrastructure of IC manufacturers' factories, providing the basis for assessing the investment into VM. The basic assumptions for the calculations are explained. Based on the scenario of implementing VM into plasma etchers of a model fab, results of benefit and cost calculation are presented.

Motivation

As complexity of semiconductor manufacturing processes grows, so does the need for reliable equipment and process control, e.g., toward the implementation of wafer-to-wafer and even within-wafer control loops. One promising approach is applying virtual metrology techniques. VM allows for controlling the process at wafer level without using the standard metrology steps. Up to now, VM algorithms have been developed; however, they are still far from being state-of-the-art in semiconductor fabs. On the one hand, VM algorithms must be tested before they are implemented into the fab information and control systems. On the other hand, the investment into VM algorithms must be evaluated and justified to be eventually adopted.

Economic Effects of VM

The implementation of VM promises to yield two main effects[1,2]: Firstly, it reduces the amount of real measurement equipment because equipment or sensor data can be used to derive the process results instead of measuring the physical properties of the processed wafers. Secondly, it reduces the number of wafers that are processed out of spec because the control loops can be very short and the process results for virtually every wafer are "controlled," in contrast to the actual measurement of only a fraction of all processed wafers.

In addition to these main effects, the application of VM is also expected to improve the utilization of process equipment because feedback loops are very short when the waiting time for the results from physical measurements is avoided. VM also improves the cycle time when fewer wafers are measured at the metrology equipment stage.

Quantification of Benefits and Costs

We calculated the potential benefits and savings due to the implementation of VM based on the aforementioned economic effects. The calculations were performed for a 200 mm wafer fab of the 0.13 µm technology node using fab and equipment data from published reports.[3-5] Furthermore, we used several assumptions for our calculations:

- Each metrology step that is not performed on a wafer saves the cost of ownership for this particular metrology step.
- The number of wafers processed with lower device yield is smaller because there is only a short delay time in noticing that the process is out of spec. The costs for this additional output are saved.
- Early warning of equipment deviations from specified performance reduces the number of wafers that must be scrapped or reworked.
- The amount of productive time for the process equipment is (slightly) increased due to less waiting time for process results from metrology steps. This time is used to produce more

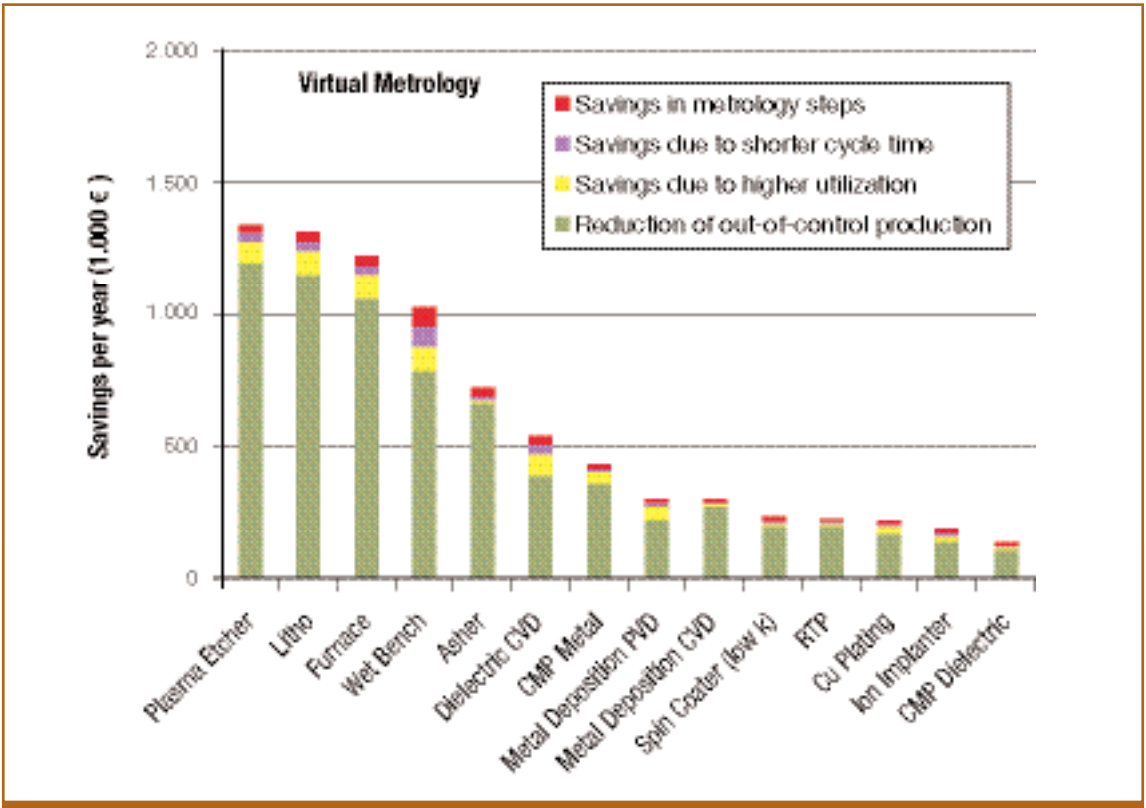

Figure 1. Potential Savings Due to the Implementation of VM for Various Equipment Types in a Model Fab

wafers and saves investment in additional equipment.
- Each metrology step that is not performed saves cycle time. Cycle time improvements reduce the capital costs for wafers that are in the fab.

The above was discussed with IC manufacturers who agreed with the assumptions. The results of these benefit calculations are shown in Figure 1 for various process equipment types.

Workshops with IC manufacturers identified and quantified the following major cost contributors for the implementation of VM: licenses for the deployment of VM algorithms; capital costs; expenses for IT-specific hardware; training material, instruction and training; manpower for rollout and implementation; manpower for improvements during pilot phase; equipment integration adaptations; embedding the VM software into the existing IT infrastructure; provision of interfaces to target systems; and purchase and integration of additional sensors.

It is assumed that VM will be implemented in the fab for a certain group of process equipment (plasma etchers) in a one-year project. Investment into VM algorithms, IT hardware and software as well as additional sensors will be depreciated over time. Costs for the first year will be higher than for the following years. It was also assumed that the full benefits from applying VM will be approached over one year of learning and improving the algorithms.

Figure 2 shows the quarterly development of cumulated benefits and costs due to the implementation of VM for the plasma etchers in the model fab.

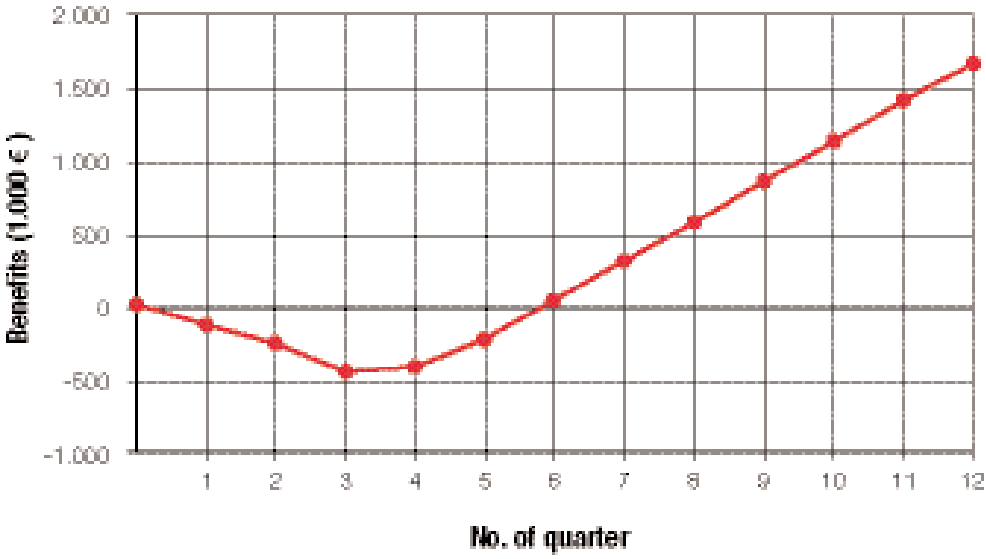

Figure 2. Cumulated Result Per Quarter Due to the Implementation of VM into Plasma Etch Equipment of a Model Fab

Evaluation of Results

As can be seen from the results of the economic benefits of VM (Figure 1), the highest contribution is due to a higher yield of the processed wafers. Depending on the type of equipment in which VM is implemented, savings due to higher utilization and savings in metrology steps can also play a role.

The calculations of costs and benefits serve as the basis for the development of models for calculating economic figures, e.g., RoI. Figure 2 depicts the temporal evolution of cumulated costs and benefits according to our model. The break-even for applying VM to all plasma etchers of the model fab will be reached within 1 1/2 years. The economic benefits from this investment balance all the associated costs after this time. After 1 1/2 years, the investment leads to a positive return for the company.

More sophisticated calculations of economic figures are currently performed. The model is also checked for the sensitivity of the calculation results to our assumptions.

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Acknowledgments

This work was funded by the EU-project IMPROVE, contract no. 120005.

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Matthias Koitzsch has been a research scientist with Fraunhofer IISB since 2006. He is active in the areas of technology development for the microelectronics industry and return on investment calculations. He holds a diploma in electrical engineering from the Friedrich-Alexander University of Erlangen-Nuremberg.

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