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Prospects for the Realization of APC in a Distributed 300 mm R&D-Line

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Motivation

Europe has the institutional and industrial centres of excellence to provide nodes for an advanced 300 mm CMOS R&D process line to implement the next technology generations below 65 nm

Within the Flying Wafer Project, funded within the 6th Framework Programme of the European Commission, specifications necessary to interlink the European R&D capabilities in a distributed 300 mm R&D-line by an effective wafer exchange concept were elaborated including

- wafer/carrier handling, monitoring, and logistics
- I/O-procedures and contamination control
- standardization of data interfaces and secure data access
- process flow planning including alternative scenarios for redundancy set-up

The Central Planning and Control System (CPCS) for wafer and process logistics which was developed within the project provides large prospects for the realization of standard compliant APC in a distributed 300 mm R&D-line

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Process distribution using a Central Planning and Control System (CPCS) – Allocation of process modules, data, and wafer exchange

Wafers are exchanged between the R&D fabs for processing in one or several process modules

Process modules are selectable from an e-catalogue and consist of a sequence of single process steps

Wafers are transferred using predefined standard compliant I/O procedures

Process and logistic data is transferred and made accessible using a Central Planning and Control System (CPCS)

Wafer/carrier tracking
Joint Data base
e-catalogue
Process flow generator
CPCS
Data
Firewall
Firewall
Firewall
R&D Fab 1
R&D Fab 2
R&D Fab 3
Wafer / Carrier

Input	Process Modules	Output
	• Gate deposition • Channel Implant • STI • **Lithography** • Etch • etc.	

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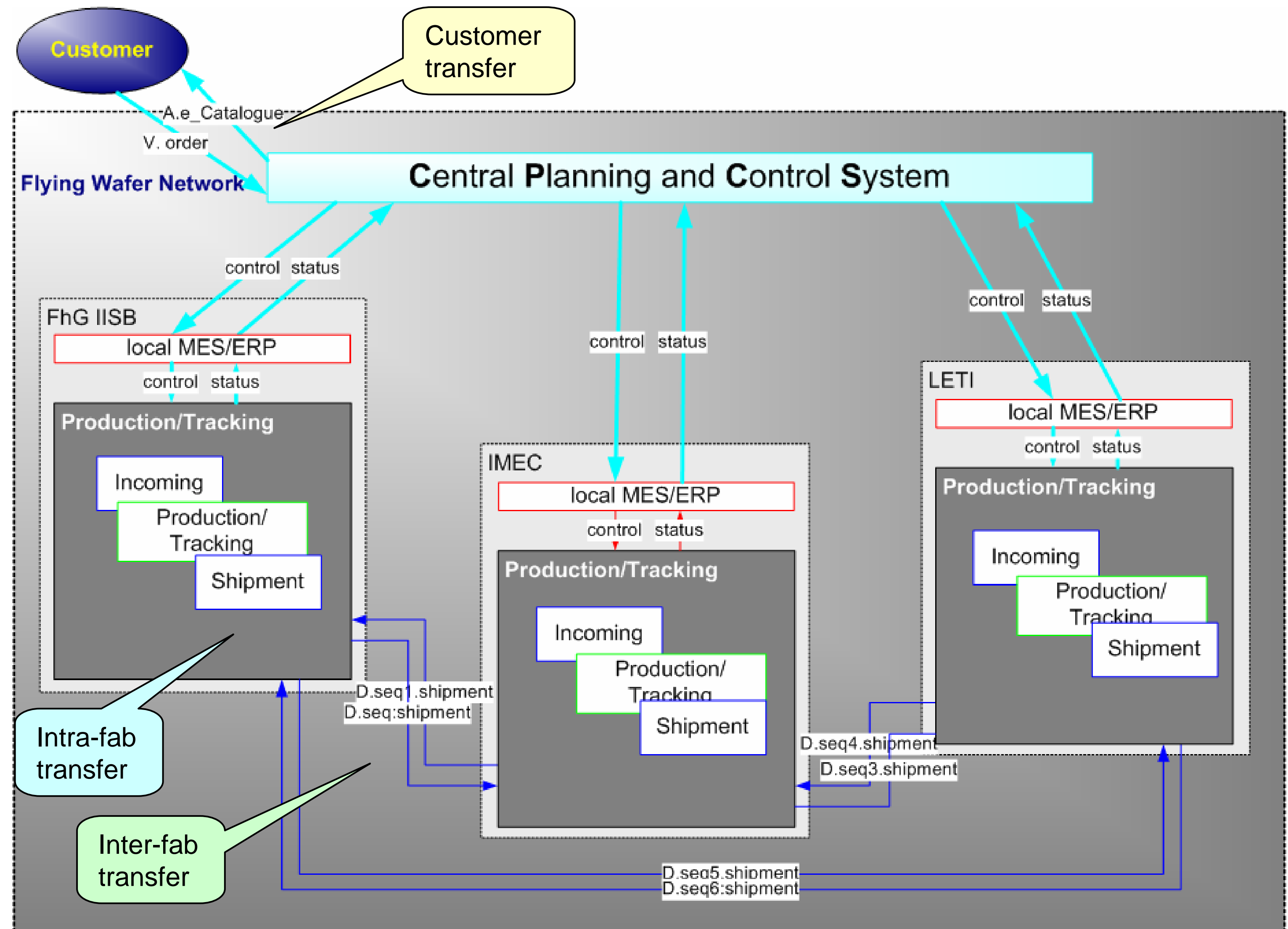
Process distribution using a Central Planning and Control System (CPCS) – Flying Wafer Network – process flow overview

Transfer Categories

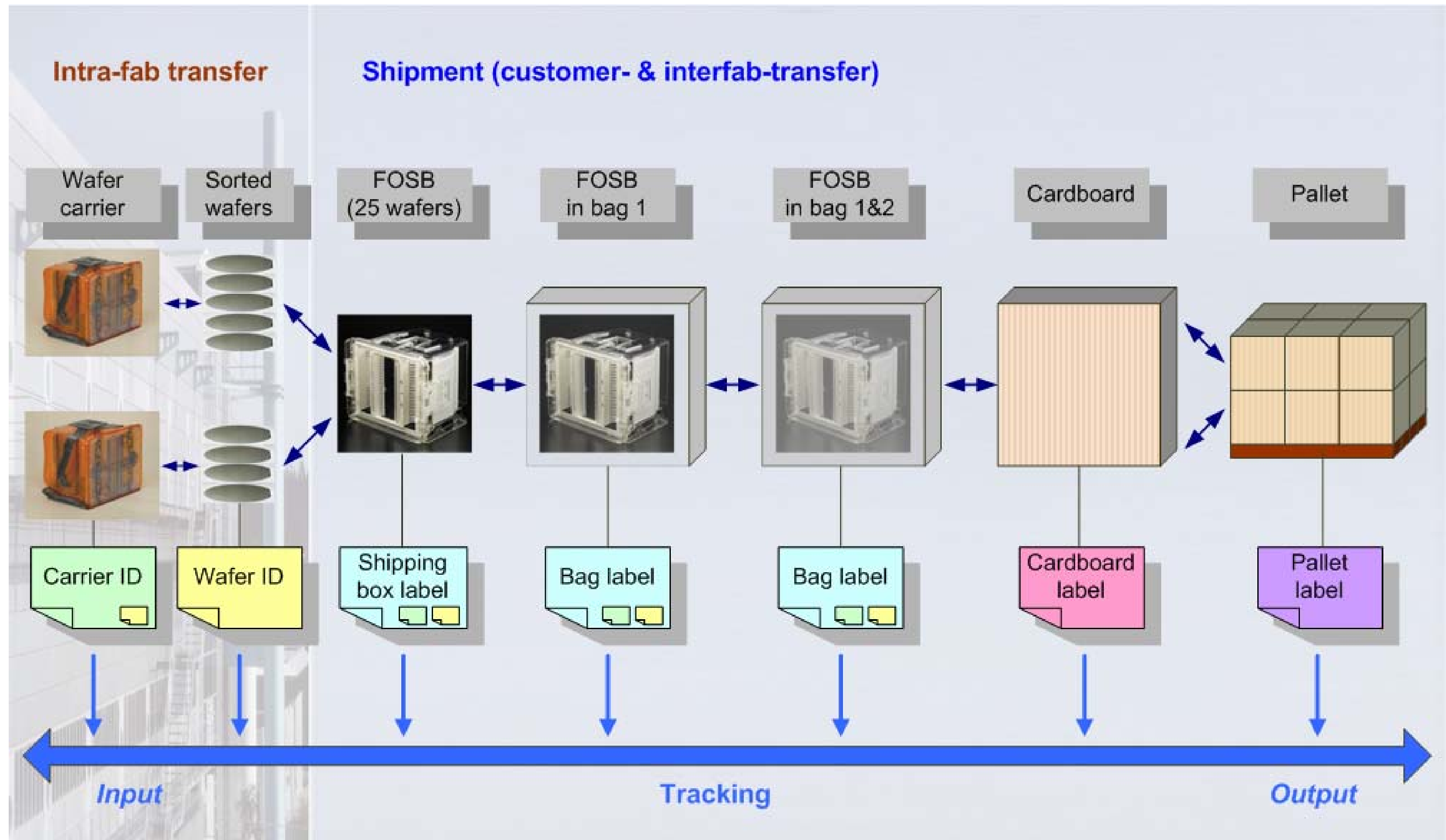
- **Customer transfer**: Transport between customer and Flying Wafer Network
- **Inter-fab transfer**: Transport between different sites within the Flying Wafer Network
- **Intra-fab transfer**: Transport within one Flying Wafer Network partner's site
- **Shipment:** Customer and inter-fab transfer which requires secondary packaging



Process distribution using a Central Planning and Control System (CPCS) – I/O and labeling procedures for wafer tracking during intra-fab transfer and shipment

Standard compliant labels

- Wafer ID
- Carrier ID
- Shipping box label
- Bag label
- Cardboard label
- Pallet label



A key aspect of the Flying Wafer network is, that tracking can be performed at wafer level. In the CPCS, the current wafer status and the wafer history may be uniquely accessed based on standard compliant wafer ID, carrier ID, and slot number.

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Relevant APC elements and SEMI standards

Process Control Systems (PCS, SEMI E133)
→ **Capabilities of functional groups, common interfaces, and data structures**

Data base systems
- Product and process logistics
- Process and equipment data
- Quality and yield data

Customer and Inter-Fab Transfer:
Provided by Flying Wafer CPCS infrastructures

Intra-Fab Transfer:
SECS/GEM (SEMI E5, SEMI E30)
→ **slow, low throughput, single-point connectivity**

Interface A (SEMI PR8, SEMI E121, SEMI125, …)
→ **fast, high throughput, multi-point connectivity, self-description (easier integration)**

Analysis Engines: R2R, SPC, FDC

Data-base

Communication infrastructure

Control action

Process

Data

Metrology

Equipment Quality Information Parameters (EQIP, SEMI E126)
→ **Run-to-run enabling standard**

Data Quality (SEMI Doc #3652A)
→ **Control actions are only as good and reliable as the data that they are based on**

Metrology integration, communication, and data (SEMI E131, SEMI E127, SEMI E141)
→ **Basis for reliable process data**

Object model

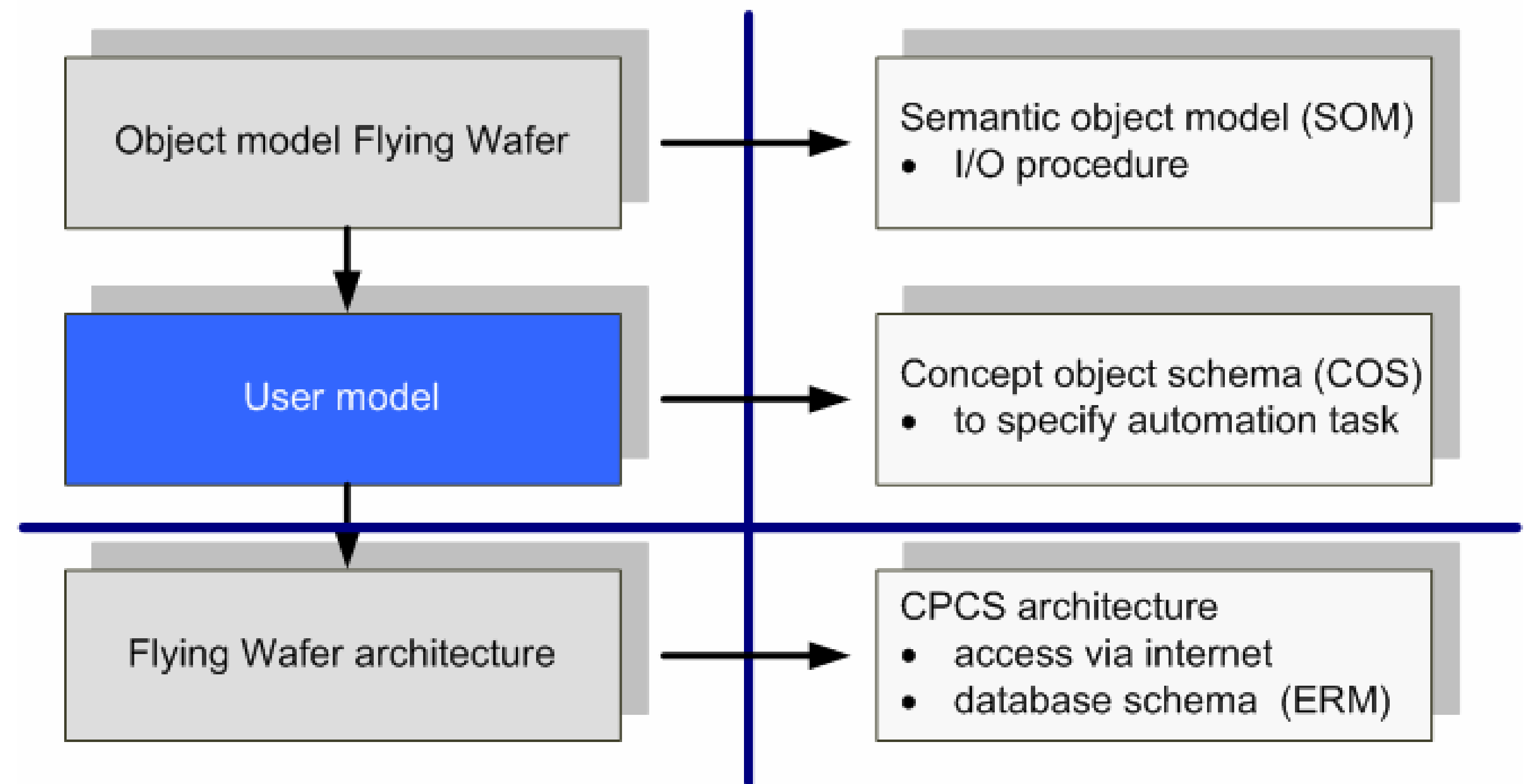
- Semantic design of all required transactions, communications, and physical tasks

User model

- Definition of all tasks and communications which can be automated between the objects of Flying Wafer

Flying wafer architecture

- Definition and usage of classes for software implementation of the CPCS architecture to provide world-wide access to tracking data via the internet



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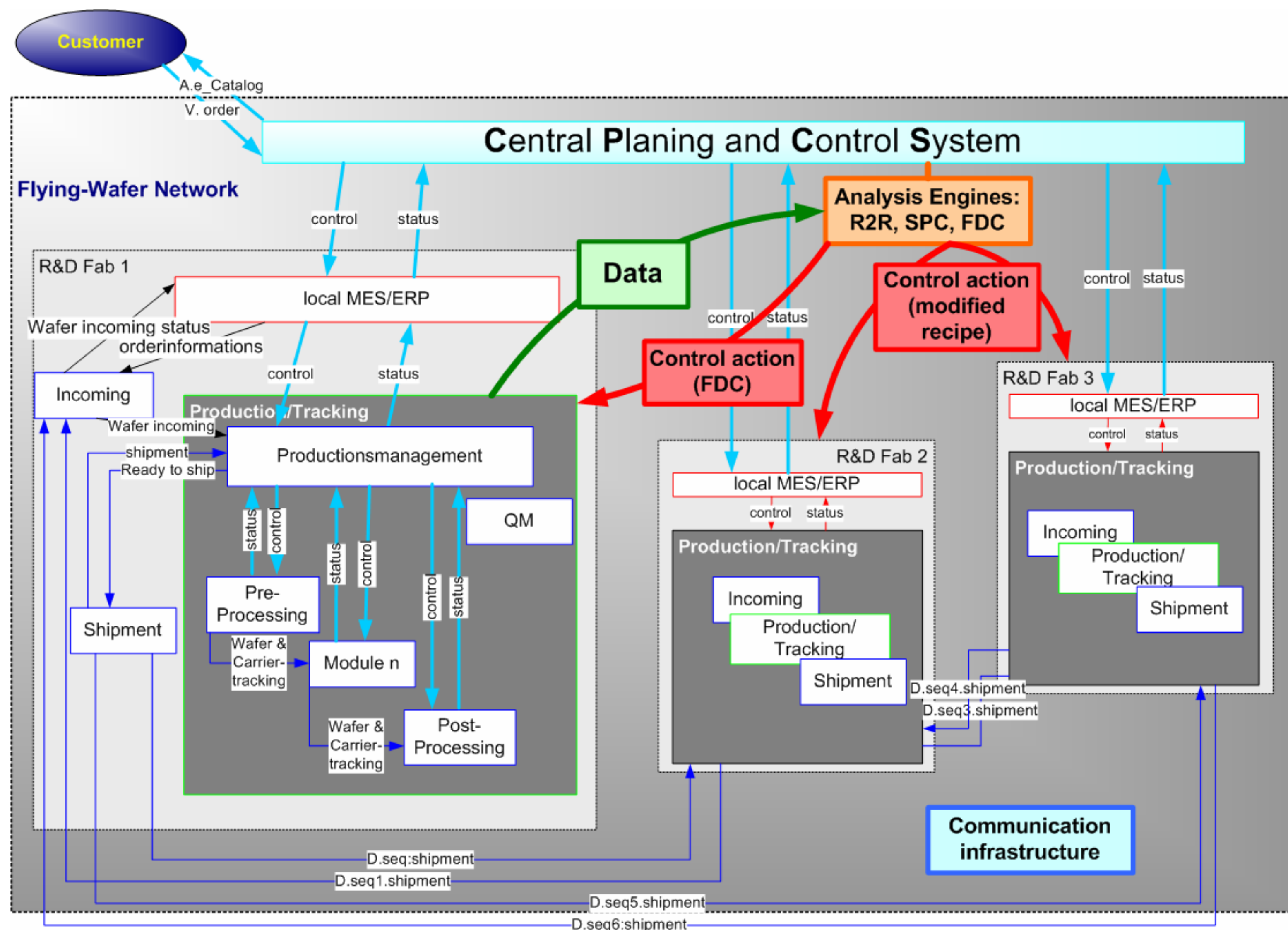
Integration of APC methods in the CPCS interaction scheme

Proposed concept

- The Central Planning and Control System (CPCS) for wafer and process logistics is based on single-wafer tracking
- Due to the single-wafer tracking approach in the CPCS, all logistic and process data is uniquely accessible for APC
- APC elements within the CPCS will complement existing fab-internal APC methods
- Relevant standard compliant APC methods can be implemented in the CPCS



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Process control example - process sequence and APC response

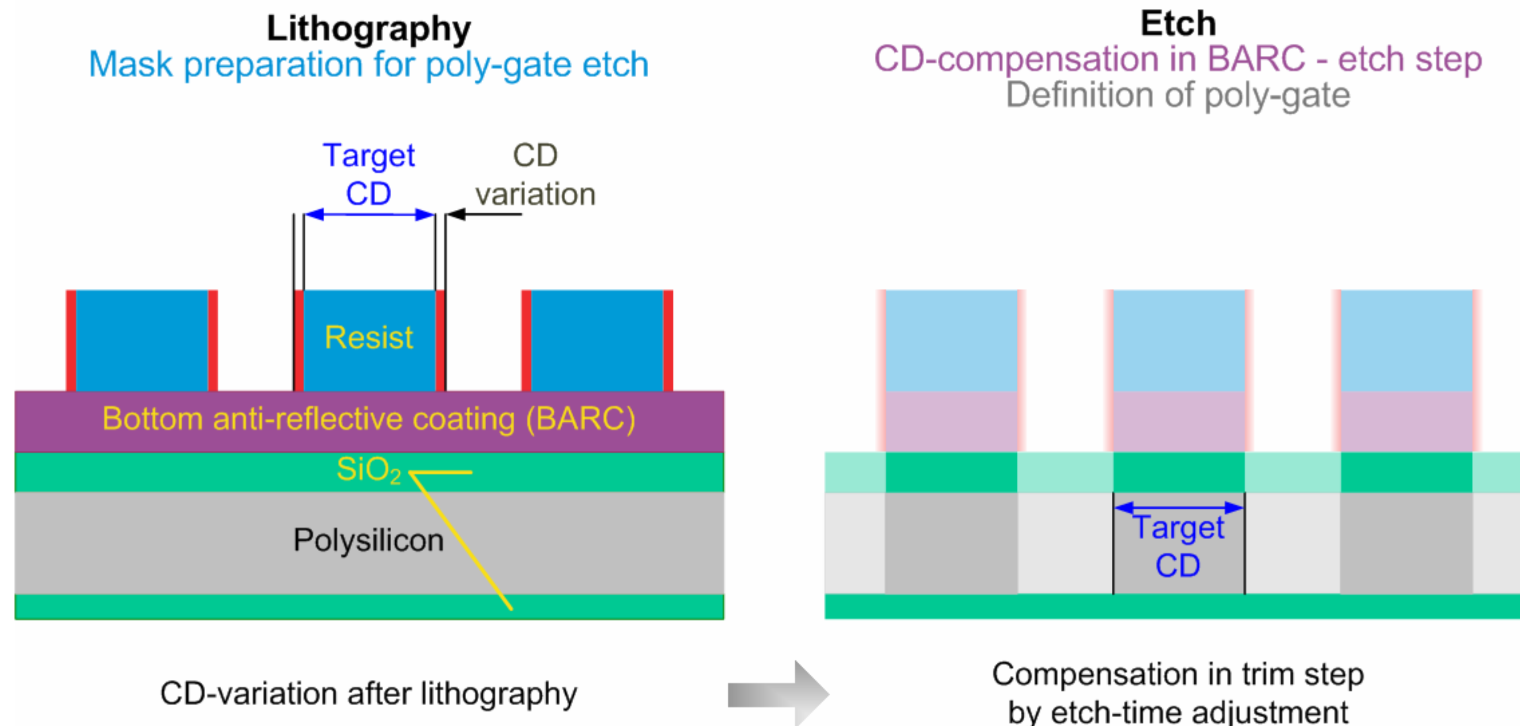
Example process sequence

Lithography and CD measurement

- Wafer exposure at stepper and resist development
- Wafer move to CD SEM; CD measurement; data transfer to APC system
- Stepper equipment data transfer to APC system
- Analysis of process data in the APC system

Etch

- Wafer move to BARC-etch equipment; etch equipment; selection of allocated BARC-etch recipe
- BARC-etch and definition of poly-gate

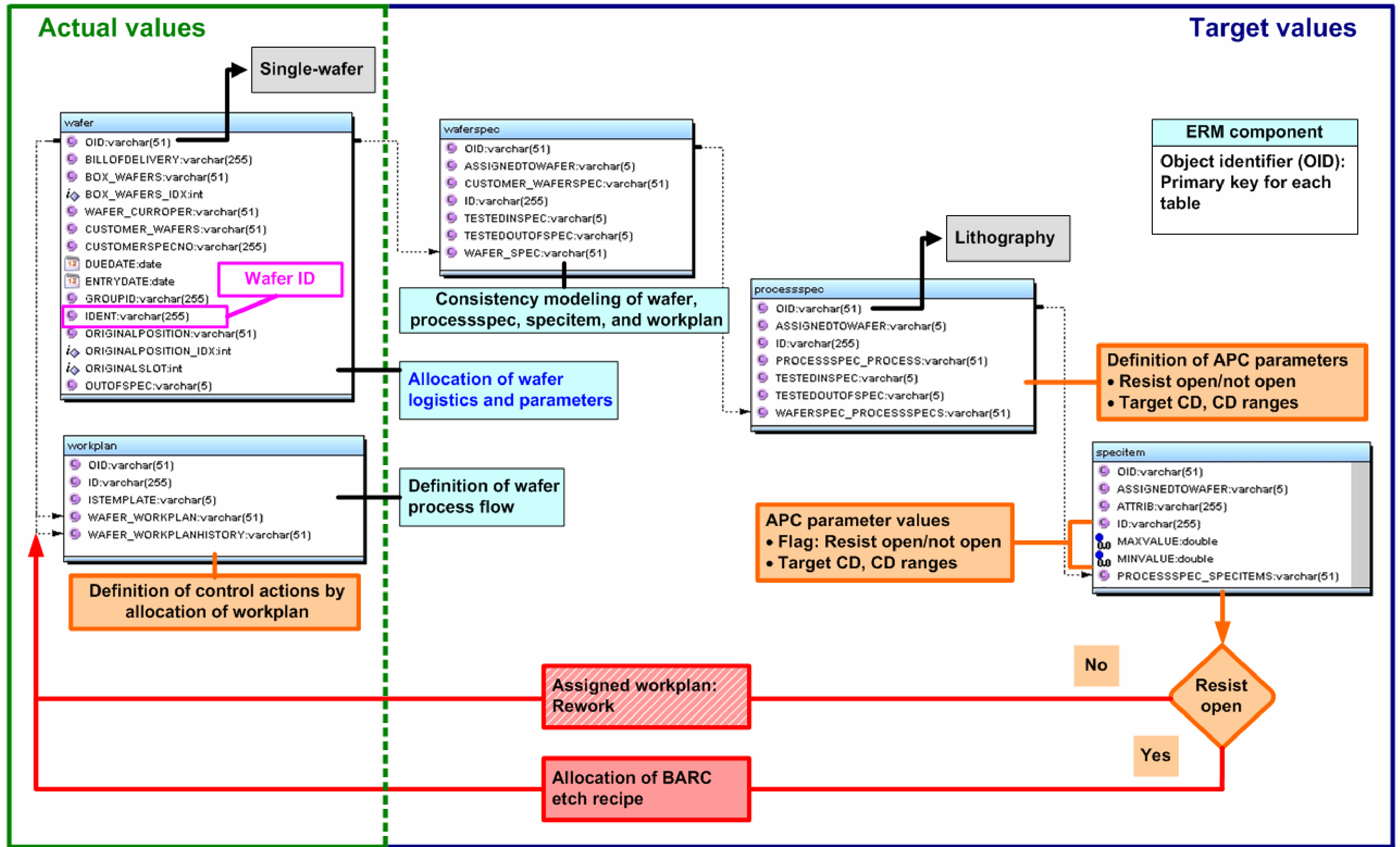


Example APC response

- FDC: Analysis of resist open/not open; analysis if rework is necessary
- Run-to-run control: Allocation of BARC-etch time depending on CD

Process control example –

Components of the Entity Relation Model (ERM) for the implementation of the process control example



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Conclusions

Within the Flying Wafer Project, a concept to implement a distributed European 300mm R&D-line was developed

A Central Planning and Control System (CPCS) was designed as core system, to provide the functionalities required for distributed wafer processing

Although the consideration of APC methodologies was not a major task during the development of the CPCS concept, its flexible design and the approach of single-wafer tracking enable the implementation of relevant APC elements

In this presentation, an approach to realize APC in the CPCS is discussed for a process example emphasizing the capability to implement APC in a distributed R&D-line